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1 **Switching Plan for a Cellular Mobile Telephone System**
*Fluhr, Z.; Nussbaum, E.;*
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 21 , Is 11 , Nov 1973
Pages:1281 - 1286

[Abstract] [PDF Full-Text (632 KB)] IEEE JNL

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2 **A router architecture for real-time communication in multicomputer networks**
*Rexford, J.; Hall, J.; Shin, K.G.;*
Computers, IEEE Transactions on , Volume: 47 , Issue: 10 , Oct. 1998
Pages:1088 - 1101

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*Wai-Hoi Wong; Hu, G.; Zhang, N.; Uribe, J.; Wang, J.; Li, H.; Lu, W.; Hossain Baghaei; Yokoyama, S.;*
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Pages:1291 - 1296

[Abstract] [PDF Full-Text (580 KB)] IEEE JNL

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*Fengjing Qiu; Starzyk, J.A.; Ying-Wei Jan;*
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*Tse Min Chen; Luo, R.C.;*

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# Switching Plan for a Cellular Mobile Telephone System

Fluhr, Z. Nussbaum, E.
Bell Laboratories, Naperville, IL, USA

*This paper appears in:* **Communications, IEEE Transactions on [legacy, pre - 1988]**

Publication Date: Nov 1973
On page(s): 1281 - 1286
Volume: 21 , Issue: 11
ISSN: 0096-2244

**Abstract:**
Federal Communication Commission **Docket** 18 262 allocated a 75-MHz band to the common carriers to implement high capacity mobile telephone systems. The Bell System has proposed a cellular arrangement of low-power transmitters/receivers that permits frequency reuse in a coverage area. This method of achieving spectrum efficiency will require extensive centralized coordination and control to properly administer channel assignments and to interconnect the mobiles with each other and with the direct distance dialing (DDD) network. This can be accomplished by means of an electronic **switching** system (ESS) with special data terminals and trunking arrangements, and a unique program. In the proposed plan the radio sites (base stations) act effectively as remote concentrators in the frequency domain under the control of ESS, which in turn acts primarily as a trunk-to-trunk **switcher.** In addition to the usual **switching,** signaling, and supervising functions, the **switching** office must also perform numerous special

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functions including paging of mobiles, location of mobiles (signal strength and ranging data analysis), channel reassignment of mobiles, and reswitching of mobiles to various base stations-these last three occurring while customers are talking.

**Index Terms:**

Bell Telephone System Mobile radio systems Telephone **switching** systems

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# A router architecture for real-time communication in multicomputer networks

Rexford, J. Hall, J. Shin, K.G.
Network & Distributed Syst., AT&T Bell Labs., Florham Park, NJ, USA;
*This paper appears in:* **Computers, IEEE Transactions on**

Publication Date: Oct. 1998
On page(s): 1088 - 1101
Volume: 47 , Issue: 10
ISSN: 0018-9340
Reference Cited: 42
CODEN: ITCOB4
Inspec Accession Number: 6087354

**Abstract:**
Parallel machines have the potential to satisfy the large computational demands of real-time applications. These applications require a predictable communication network, where time-constrained traffic requires bounds on throughput and latency, while good average performance suffices for best-effort packets. This paper presents a new router architecture that tailors low-level routing, **switching**, arbitration, flow-control, and deadlock-avoidance policies to the conflicting demands of each traffic class. The router implements bandwidth regulation and deadline-based scheduling, with packet **switching**

and table-driven multicast routing, to bound end-to-end delay and buffer requirements for time-constrained traffic while allowing best-effort traffic to capitalize on the low-latency routing and **switching** schemes common in modern parallel machines. To limit the cost of servicing time-constrained traffic, the router includes a novel packet scheduler that shares link-scheduling logic across the multiple output ports, while masking the effects of **dock** rollover on the representation of packet eligibility times and deadlines. Using the Verilog hardware description language and the Epoch silicon compiler, we demonstrate that the router design meets the performance goals of both traffic classes in a single-chip solution. Verilog simulation experiments on a detailed timing model of the chip show how the implementation and performance properties of the packet scheduler scale over a range of architectural parameters

**Index Terms:**
multiprocessor interconnection networks packet **switching** parallel architectures performance evaluation real-time systems Epoch silicon compiler Verilog hardware description language Verilog simulation architectural parameters buffer requirements deadline-based scheduling end-to-end delay latency multicomputer networks packet **switching** parallel machines predictable communication network real-time applications real-time communication router architecture table-driven multicast routing throughput time-constrained traffic



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